THE INVENTION CLAIMED IS:

1. An apparatus for determining doping concentration of a semiconductor wafer comprising:

a probe having an electrically conductive tip and an electrical insulator covering at least a distal end of the conductive tip;

means for applying a capacitance-voltage (CV) type electrical stimulus between the electrically conductive tip and a semiconductor wafer when the electrical insulator is in contact with the semiconductor wafer;

means for measuring a CV response of the semiconductor wafer to the CV type electrical stimulus; and

means for determining from the CV response a doping concentration of the semiconductor wafer.

2. The apparatus as set forth in claim 1, wherein:

the electrical insulator contacts a surface of the semiconductor wafer; and

the doping concentration is determined for a near surface region of the semiconductor wafer adjacent the electrical insulator.

3. The apparatus as set forth in claim 1, wherein the carriers are one of P-type carriers and N-type carriers.

4. The apparatus as set forth in claim 1, wherein the electrical insulator surrounds the electrically conductive tip and at least part of a shaft of the probe adjacent the electrically conductive tip.

5. The apparatus as set forth in claim 1, wherein contact between the electrical insulator and the semiconductor wafer forms a Metal-Oxide-Semiconductor (MOS) type junction, where the electrically conductive tip is the metal, the electrical insulator functions in the same manner as an oxide layer and the semiconductor wafer is the semiconductor.

6. The apparatus as set forth in claim 1, wherein the measuring means measures the CV response to within one Debye length from the interface of the electrical insulator and the semiconductor wafer.

7. The apparatus as set forth in claim 1, wherein at least the electrically conductive tip is formed from an elastically deformable material.

8. The apparatus as set forth in claim 1, wherein the electrical insulator contacts one of (i) a semiconductor material of the semiconductor wafer and (ii) a dielectric or oxide layer overlaying the semiconductor material.